formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-40 are presently active. Claims 1-40 have been amended by the present amendment. The changes to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claims 1-3, 11-13, 21-23, and 31-33 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,973,338 to Okabe et al. (hereinafter "the '338 patent"); Claims 4, 14, 24, and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '338 patent, further in view of U.S. Patent No. 6,300,663 to Kapoor (hereinafter "the '663 patent"); Claims 5, 15, 25, and 35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '338 patent; and Claims 6-10, 16-20, 26-30, and 36-40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '338 and '663 patents, further in view of U.S. Patent No. 6,331,466 to Takahashi et al.

Amended Claim 1 is directed to a power semiconductor device comprising, inter alia: (1) a base layer of a first conductivity type, (2) a base layer of a second conductivity type selectively formed on one surface of the base layer of the first conductivity type, (3) an emitter layer of the first conductivity type selectively formed on the surface of the base layer of the second conductivity type, (4) a gate insulating film formed on a surface of the base layer of the second conductivity type that lies between the emitter layer and the base layer of the first conductivity type, the gate insulating layer film including a first insulating portion

and a second insulating portion, and (5) a gate electrode formed above the gate insulating film. Claim 1 has been amended to clarify that (1) the gate electrode is formed *above* the gate insulating film and (2) the capacitance of a capacitor formed of the second insulating portion is smaller than the capacitance of a capacitor formed of the first insulating portion. The changes to the claims are supported by the originally filed specification and do not add new matter.[2]

Applicants respectfully submit that the rejection of Claims 1-3 as anticipated by the '338 patent is rendered moot by the present amendment to Claim 1.

The '338 patent is directed to an insulating gate type bipolar transistor (IGBT). Figure 6 of the '338 patent discloses a gate electrode 63 surrounded by an insulating film. However, the '338 patent fails to disclose a gate insulating film formed on a surface of the base layer of the second conductivity type that lies between an emitter layer and the base layer of the first conductivity type, wherein (1) the gate insulating film includes a first insulating portion and a second insulating portion, (2) a gate electrode is formed above the gate insulating film, and (3) the capacitance of a capacitor formed on the second gate insulating portion is smaller than a capacitance of a capacitor formed of the first insulating portion, as recited in amended Claim 1. Accordingly, Applicants respectfully submit that Claims 1-3 patentably define over the '338 patent.

Regarding the rejections of Claims 4-10 under 35 U.S.C. § 103, Applicants respectfully submit that the '663 and '466 patents fail to remedy the deficiencies of the '338 patent with regard to the claimed gate electrode and gate insulating film, as discussed above.

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[2]See, for example, Figure 1.

Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejections of Claims 4-10 should be withdrawn.

Independent Claims 11, 21, and 31 recite limitations analogous to the limitations recited in amended Claim 1. Moreover, those claims have been amended to reflect the present amendment to Claim 1. Thus, for the reasons stated above for the patentability of Claim 1, Applicants respectfully submit that the rejections of independent Claims 11-13, 21-23, and 31-33 as anticipated by the '338 patent are rendered moot by the present amendment of Claims 11, 21, and 31, respectively.

Further, for the reasons set forth above for the patentability of Claims 4-10, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of dependent Claims 14-20, 24-30, and 34-40 be withdrawn.

The present amendment is submitted in accordance with the provisions of 37 C.F.R. §1.116, which after Final Rejection permits entry of amendments placing the claims in better form for consideration on appeal. As the present amendment is believed to overcome outstanding rejections under 35 U.S.C. §§ 102 and 103, the present amendment places the application in better form for consideration on appeal. It is therefore respectfully requested that 37 C.F.R. §1.116 be liberally construed, and that the present amendment be entered.

Thus, it is respectfully submitted that Claim 1 (and dependent Claims 2-10), Claim 11 (and dependent Claims 12-20), Claim 21 (and dependent Claims 22-30), Claim 31 (and dependent Claims 32-40) patentably define over the '338, '663, and '466 patents.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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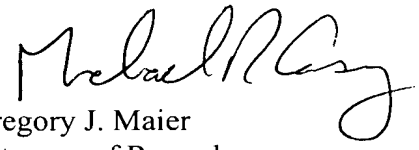

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IN THE CLAIMS

1. (Three Times Amended) A power semiconductor device comprising:

a base layer of a first conductivity type;

a base layer of a second conductivity type selectively formed on one surface of said base layer of the first conductivity type;

an emitter layer of the first conductivity type selectively formed on the surface of said base layer of the second conductivity type;

a collector layer selectively formed on one of the one surface and another surface of said base layer of the first conductivity type;

a first main electrode formed on said collector layer;

a second main electrode formed on said emitter layer and on said base layer of the second conductivity type; [and]

a gate [electrode formed with first and second gate insulating films on] insulating film formed on a surface of said base layer of the second conductivity type that lies between said emitter layer and said base layer of the first conductivity type, said gate insulating film including a first insulating portion and a second insulating portion; and

a gate electrode formed above said gate insulating film,

wherein a capacitance of a capacitor formed [on] of the second [gate] insulating [film] portion is [different from] smaller than a capacitance of a capacitor formed [on] of the first [gate] insulating [film] portion.

2. (Three Times Amended) The power semiconductor device according to claim 1, wherein the first [gate] insulating [film] portion is formed in a portion near said emitter layer, and the second [gate] insulating [film] portion is formed in a portion near said base layer of the first conductivity type.

3. (Twice Amended) The power semiconductor device according to claim 2, wherein a thickness of the second [gate] insulating [film] portion is larger than a thickness of the first [gate] insulating [film] portion.

4. (Twice Amended) The power semiconductor device according to claim 2, wherein a dielectric constant of the second [gate] insulating [film] portion is smaller than a dielectric constant of the first [gate] insulating [film] portion.

5. (Three Times Amended) The power semiconductor device according to claim 2, wherein a thickness of the second [gate] insulating [film] portion has an inclination and the thickness thereof on a side of said emitter layer is smaller than a thickness on a side of said base layer of the first conductivity type.

6. (Three Times Amended) The power semiconductor device according to claim 1, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films]

portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

7. (Three Times Amended) The power semiconductor device according to claim 2, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

8. (Three Times Amended) The power semiconductor device according to claim 3, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

9. (Three Times Amended) The power semiconductor device according to claim 4, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

10. (Three Times Amended) The power semiconductor device according to claim 5, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films]

portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

11. (Three Times Amended) A method of manufacturing a power semiconductor device comprising:

forming a base layer of a first conductivity type;

selectively forming a base layer of a second conductivity type on one surface of the base layer of the first conductivity type;

selectively forming an emitter layer of the first conductivity type on a surface of the base layer of the second conductivity type;

selectively forming a collector layer on one of the one surface and another surface of the base layer of the first conductivity type;

forming a first main electrode on said collector layer;

forming a second main electrode on said emitter layer and on the base layer of the second conductivity type; [and]

forming [first and second] a gate insulating film[s] on a surface of the base layer of the second conductivity type that lies between said emitter layer and the base layer of the first conductivity type, [and forming a] said gate [electrode on the] insulating film including a first insulating portion and a second [gate] insulating [films] portion; and

forming a gate electrode above said gate insulating film,

wherein a capacitance of a capacitor formed [on] of the second [gate] insulating [film] portion is [different from] smaller than a capacitance of a capacitor formed [on] of the first [gate] insulating [film] portion.

12. (Twice Amended) The method of manufacturing a power semiconductor device according to claim 11, wherein the first [gate] insulating [film] portion is formed in a portion near said emitter layer and the second [gate] insulating [film] portion is formed in a portion near said base layer of the first conductivity type.

13. (Amended) The method of manufacturing a power semiconductor device according to claim 12, wherein a thickness of the second [gate] insulating [film] portion is larger than a thickness of the first [gate] insulating [film] portion.

14. (Amended) The method of manufacturing a power semiconductor device according to claim 12, wherein a dielectric constant of the second [gate] insulating [film] portion is smaller than a dielectric constant of the first [gate] insulating [film] portion.

15. (Twice Amended) The method of manufacturing a power semiconductor device according to claim 12, wherein a thickness of the second [gate] insulating [film] portion has an inclination and the thickness thereof on a side of said emitter layer is smaller than a thickness on a side of said base layer of the first conductivity type.

16. (Twice Amended) The method of manufacturing a power semiconductor device according to claim 11, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

17. (Twice Amended) The method of manufacturing a power semiconductor device according to claim 12, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

18. (Twice Amended) The method of manufacturing a power semiconductor device according to claim 13, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

19. (Twice Amended) The method of manufacturing a power semiconductor device according to claim 14, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

20. (Twice Amended) The method of manufacturing a power semiconductor device according to claim 15, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said emitter layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

21. (Amended) A power semiconductor device comprising:

a base layer of a first conductivity type;

a base layer of a second conductivity type selectively formed on one surface of said base layer of the first conductivity type;

a source layer of the first conductivity type selectively formed on the surface of said base layer of the second conductivity type;

a drain layer selectively formed on one of the one surface and another surface of said base layer of the first conductivity type;

a first main electrode formed on said drain layer;

a second main electrode formed on said source layer and on said base layer of the second conductivity type; [and]

a gate [electrode formed with first and second gate insulating films on] insulating film formed on a surface of said base layer of the second conductivity type that lies between said source layer and said base layer of the first conductivity type, said gate insulating film including a first insulating portion and a second insulating portion; and

a gate electrode formed above said gate insulating film,

wherein a capacitance of a capacitor formed [on] of the second [gate] insulating [film] portion is [different from] smaller than a capacitance of a capacitor formed [on] of the first [gate] insulating [film] portion.

22. (Amended) The power semiconductor device according to claim 21, wherein the first [gate] insulating [film] portion is formed in a portion near said one of said source layer, and the second [gate] insulating [film] portion is formed in a portion near said base layer of the first conductivity type.

23. (Amended) The power semiconductor device according to claim 22, wherein a thickness of the second [gate] insulating [film] portion is larger than a thickness of the first gate insulating film.

24. (Amended) The power semiconductor device according to claim 22, wherein a dielectric constant of the second [gate] insulating [film] portion is smaller than a dielectric constant of the first gate insulating film.

25. (Amended) The power semiconductor device according to claim 22, wherein a thickness of the second [gate] insulating [film] portion has an inclination and the thickness thereof on a side of said source layer is smaller than a thickness on a side of said base layer of the first conductivity type.

26. (Amended) The power semiconductor device according to claim 21, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

27. (Amended) The power semiconductor device according to claim 22, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

28. (Amended) The power semiconductor device according to claim 23, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

29. (Amended) The power semiconductor device according to claim 24, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

30. (Amended) The power semiconductor device according to claim 25, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

31. (Amended) A method of manufacturing a power semiconductor device comprising:

forming a base layer of a first conductivity type;

selectively forming a base layer of a second conductivity type on one surface of the base layer of the first conductivity type;

selectively forming a source layer of the first conductivity type on a surface of the base layer of the second conductivity type;

selectively forming a drain layer on one of the one surface and another surface of the base layer of the first conductivity type;

forming a first main electrode on the drain layer;

forming a second main electrode on the source layer of the first conductivity type and on the base layer of the second conductivity type; [and]

forming [first and second] a gate insulating film[s] on a surface of the base layer of the second conductivity type that lies between the source layer of the first conductivity type and the base layer of the first conductivity type, [and forming a] said gate [electrode on the] insulating film including a first insulating portion and a second [gate] insulating [films] portion; and

forming a gate electrode above said gate insulating film,

wherein a capacitance of a capacitor formed [on] of the second [gate] insulating [film] portion is [different from] smaller than a capacitance of a capacitor formed [on] of the first [gate] insulating [film] portion.

32. (Amended) The method of manufacturing a power semiconductor device according to claim 31, wherein the first [gate] insulating [film] portion is formed in a portion near said source layer and the second [gate] insulating [film] portion is formed in a portion near said base layer of the first conductivity type.

33. (Amended) The method of manufacturing a power semiconductor device according to claim 32, wherein a thickness of the second [gate] insulating [film] portion is larger than a thickness of the first [gate] insulating [film] portion.

34. (Amended) The method of manufacturing a power semiconductor device according to claim 32, wherein a dielectric constant of the second [gate] insulating [film] portion is smaller than a dielectric constant of the first gate insulating film.

35. (Amended) The method of manufacturing a power semiconductor device according to claim 32, wherein a thickness of the second [gate] insulating [film] portion has an inclination and the thickness thereof on a side of said source layer is smaller than a thickness on a side of said base layer of the first conductivity type.

36. (Amended) The method of manufacturing a power semiconductor device according to claim 31, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

37. (Amended) The method of manufacturing a power semiconductor device according to claim 32, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

38. (Amended) The method of manufacturing a power semiconductor device according to claim 33, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being

formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

39. (Amended) The method of manufacturing a power semiconductor device according to claim 34, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

40. (Amended) The method of manufacturing a power semiconductor device according to claim 35, wherein said gate electrode is buried in a trench with the first and second [gate] insulating [films] portions disposed therebetween to form a trench structure, the trench being formed to range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.